

Development of a Calibration Technique Using a Standard High-voltage Divider for the VT1005

By Shuhei Yamada, Kenichi Seki, and Makoto Muto
HIOKI E.E. Corporation

1. Introduction

As high-withstand-voltage SiC devices enter into wide use in industry^{1, 2, 3)}, it is becoming increasingly important to be able to measure power at devices carrying voltages in excess of 1 kV, for example high-voltage inverters, with a high degree of precision. To ensure the reliability of such power measurements, it is important to use instruments whose accuracy is defined for high voltages across a broad band.

Typical calibrators such as the 5730A and 5725A (Fluke) are used together, but the upper limit on the voltages they can generate is approximately 1 kV. While high-voltage voltmeters (for DC voltages) and voltage transformers (for voltages at the grid frequency of 50/60 Hz) are used for calibration at voltages in excess of 1 kV, high-accuracy (<0.1%) calibration is only possible for DC and grid-frequency voltages.

In this project, we developed a technique for fabricating a unique standard high-voltage divider and calibrating its division ratio. This device allows high-accuracy calibration for high voltages across a broad frequency band ranging from DC to 10 kHz. This paper introduces how the developed technique made it possible to supply the AC/DC High Voltage Divider VT1005 with accuracy defined for high voltages.

2. Design of the standard high-voltage divider

2.1 Divider types and designs

Types of voltage dividers include resistive voltage dividers, capacitive voltage dividers, and inductive voltage dividers. We chose a resistive voltage divider due to the requirement that it operate from DC to 10 kHz. As illustrated in Fig. 1, the standard high-voltage divider we designed consists of a resistive voltage division circuit and a buffer circuit.

2.2 Design of the resistive voltage division circuit

In the resistive voltage division circuit, the applied voltage V_{in} is attenuated according to the ratio of R_{hi} (2.2 M Ω , $i = 1 \sim 12$) and R_l (2.68 k Ω). At this point, the voltage applied to R_l is low, and its voltage dependence can be ignored. By contrast, the high voltage applied to R_{hi} means that its voltage dependence cannot be ignored. To reduce this voltage dependence, we used a metallic thin-film chip-type resistor, a type characterized by a low temperature coefficient (± 10 ppm/ $^{\circ}C$ [max.], -1.9 ppm/ $^{\circ}C$ [typ.]).

In this project, we used the standard high-voltage divider and an equivalent SPICE circuit model, as explained below. Most wide-band resistive voltage dividers have shielding to compensate for the effects of parasitic capacitance in order to lower the frequency dependence of the division ratio^{4, 5, 6, 7)}. However, the existence of an internal shield potential and the fact that the distances between individual input resistors and the internal shield result in complex parasitic capacitive coupling make it difficult to build a circuit model.

In this project, we chose a simple design without internal shielding, as shown in Fig. 2, to address this issue. Because the distances between individual input resistors R_{hi} ($i = 1 \sim 12$) and the ground potential

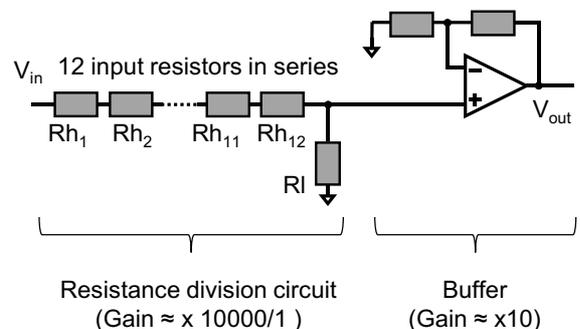


Fig. 1: Design of the standard high-voltage divider

are uniform, the input resistors share a common parasitic capacitive coupling (for example, the capacitive coupling between the resistors and ground in Fig. 2). Although the division ratio exhibits greater frequency dependence, this design provides an advantage in terms of the ease with which a highly reliable circuit model can be built thanks to its simpler capacitive coupling.

2.3 Design of the buffer circuit

If the output from the resistive voltage division circuit were connected to the instrument directly, it would be affected by the instrument's input impedance and the output cable's parasitic capacitance. To avoid these effects, we designed a buffer circuit downstream of the resistive voltage division circuit. To protect the buffer circuit from disturbances, we shielded it with a shield case and used N-type connectors for its input and output. The buffer circuit's voltage dependence is small enough that it can be ignored.

3. Standard high-voltage divider calibration method

3.1 Use of the division ratio's coefficient of variation $\delta k[V]$

As described above, the standard high-voltage divider's division ratio is likely to exhibit voltage dependence caused by the temperature and voltage coefficients of the input resistors R_{h_i} . Consequently, it is necessary to calibrate the division ratio at the applied voltage that will be used in calibration (>1 kV). As described above, the division ratio cannot be

calibrated directly due to the lack of high-accuracy calibrators that support frequencies other than DC and the grid frequency at voltages of 1 kV and higher.

To address this issue, we developed a technique for calibrating the desired division ratio $k[V]$ by calibrating the division ratio $k[1 \text{ kV}]$ for an applied voltage of 1 kV and the division ratio coefficient of variation $\delta k[V]$ at the desired applied voltage. Following is a summary of that process.

If the division ratio at an applied voltage V is expressed as $k[V]$, the division ratio coefficient of variation $\delta k[V]$ can be defined as shown in Equation (1). We used 1 kV as the standard for the division ratio coefficient of variation.

$$\delta k[V] \equiv \frac{k[V] - k[1 \text{ kV}]}{k[1 \text{ kV}]} \quad (1)$$

Equation (1) can be transformed to obtain Equation (2) below:

$$k[V] = (1 + \delta k[V]) \cdot k[1 \text{ kV}] \quad (2)$$

The desired division ratio $k[V]$ can be calibrated by calibrating $k[1 \text{ kV}]$ and $\delta k[V]$.

If the input resistance value at the applied voltage V is expressed as $R_{h_i}[V]$, the resistance value coefficient of variation $\delta R_{h_i}[V]$ can be defined as shown in Equation (3). We used 1 kV as the standard for the resistance value coefficient of variation.

$$\delta R_{h_i}[V] \equiv \frac{R_{h_i}[V] - R_{h_i}[1 \text{ kV}]}{R_{h_i}[1 \text{ kV}]} \quad (3)$$

Since the division ratio for a DC voltage is determined by the resistance value, the division ratio coefficient of variation $\delta k[V]$ and the average resistance value coefficient of variation $\delta R_{h_i}[V]$ are related as described in Equation (4). (See Appendix A.)

$$\delta k[V](\text{DC}) \approx \sum_{i=1}^{12} \frac{\delta R_{h_i}[V]}{12} \quad (4)$$

Consequently, for DC voltages, the division ratio coefficient of variation $\delta k[V]$ can be calibrated by measuring the individual resistance value coefficients of variation $\delta R_{h_i}[V]$ ($i=1$ to 12). For AC voltages, the division ratio is affected by parasitic capacitance. Consequently, the average value of $\delta R_{h_i}[V]$ and $\delta k[V]$ do not agree.

$$\delta k[V](\text{AC}) \neq \sum_{i=1}^{12} \frac{\delta R_{h_i}[V]}{12} \quad (5)$$

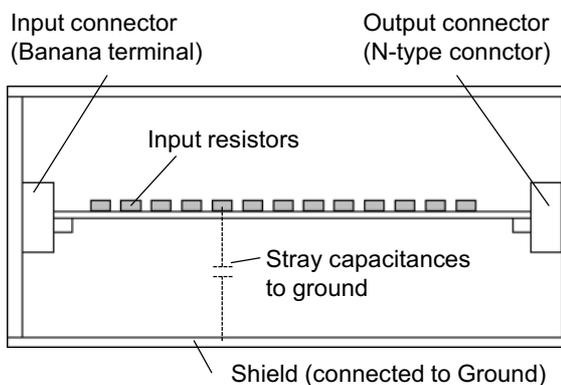


Fig. 2: Input resistor shielding

To reckon the effect of parasitic capacitance on the division ratio, we built an electronic circuit model of the standard high-voltage divider that includes parasitic capacitance, as shown in Fig. 3. We calibrated the division ratio coefficient of variation $\delta k[V]$ by substituting observed values of the resistance value coefficient of variation $\delta R_{h_i}[V]$ into the model.

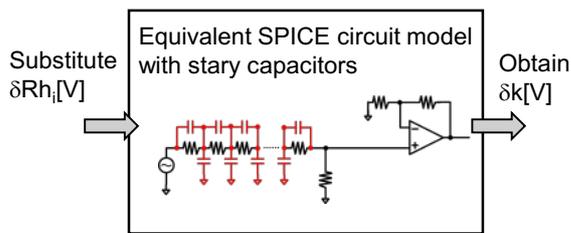


Fig. 3: Illustration of the method for calibrating division ratio fluctuation using an electronic circuit model

3.2 Creation of the electronic circuit model

Fig. 4 illustrates our electronic circuit model for the standard high-voltage divider. We described capacitance coupling between a and c, a and d, and b and d, bypassing R_{h_i} , as the parasitic capacitance affecting the division ratio. Other parasitic capacitance values were left out since their effects are small enough to be ignored.

Fig. 5 illustrates an electronic circuit model for the input resistance R_{h_i} including parasitic capacitance. The model describes the parasitic capacitance C_p between the resistor and pad, the capacitive coupling C_{pg} between the resistor pattern and ground, and the capacitive coupling C_{tg} between the resistance electrode and ground, all of which should affect division ratios for AC voltages.

Measured values were then applied to the resistance values in the circuit model. However, it is

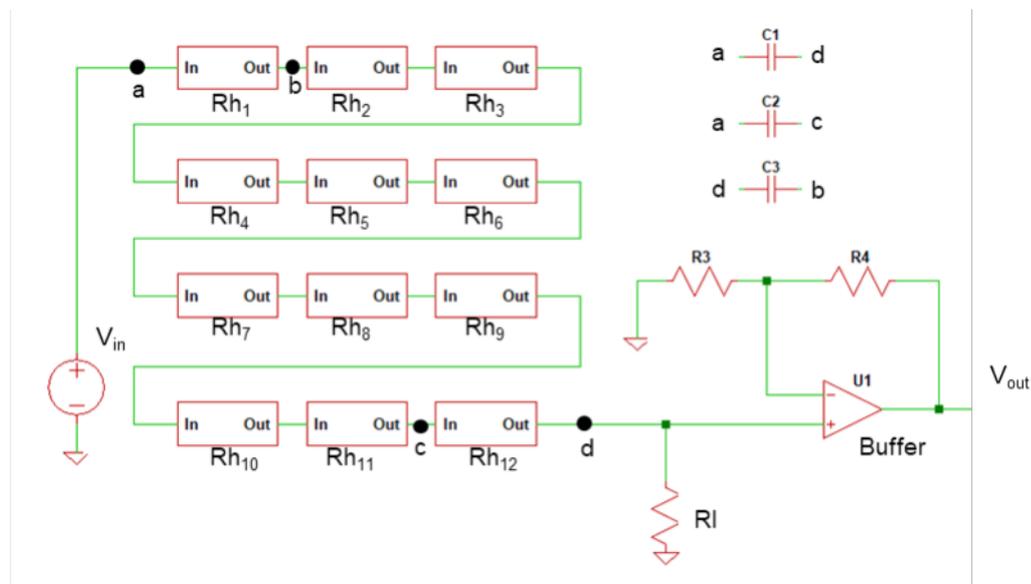


Fig. 4: Electronic circuit (SPICE) model created for the standard high-voltage divider

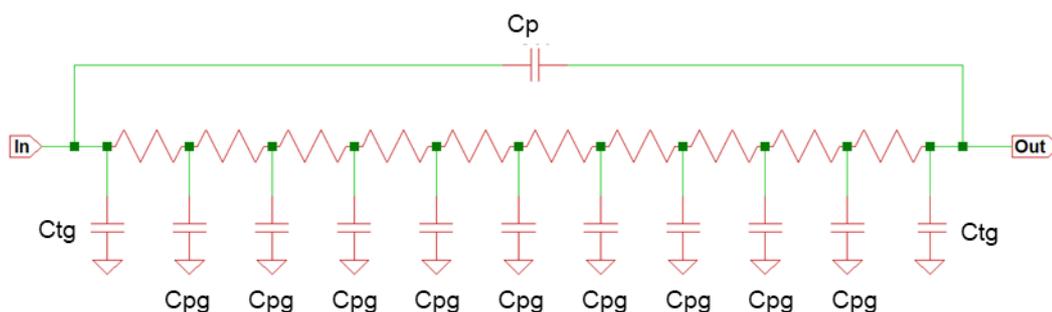


Fig. 5: Electronic circuit (SPICE) model for input resistance R_{h_i} including parasitic capacitance

difficult to measure parasitic capacitance values. To address this issue, we estimated the parasitic capacitance values by means of electromagnetic field simulation (FEMTET), searched for parasitic capacitance values that reproduced the frequency characteristics observed in the vicinity, and applied them to the circuit model.

Fig. 6 provides a comparison of the observed frequency characteristics of the standard high-voltage divider and the frequency characteristics obtained by our simulation of the electronic circuit we built. The simulated characteristics match the observed characteristics at an error of ± 20 ppm or less within the frequency range actually used in calibration (40 Hz to 10 kHz).

4. Standard high-voltage divider calibration results

4.1 Measurement of the resistance value coefficient of variation $\delta R_{h_i}[V]$

When the voltage V is applied to the standard high-voltage divider, a voltage of $V/12$ is applied across individual input resistors R_{h_i} . We mounted each input resistor R_{h_i} on a separate board designed to measure resistance values, applied a voltage of $V/12$ across it, measured the current flowing through the resistor, and used Ohm's law to calculate the resistance values $R_{h_i}[V]$ and $R_{h_i}[1\text{ kV}]$. We calculated the resistance value coefficient of variation $\delta R_{h_i}[V]$ using the calculated resistance values and Equation (3).

Voltage was generated using a 5730A, and current was measured using a 3458A (Keysight). The effects of

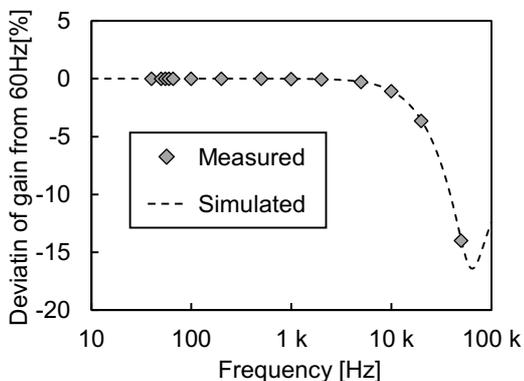


Fig. 6: Comparison of observed and analyzed frequency characteristics

parasitic resistance were eliminated during measurement by measuring the wiring resistance and the 3458A's input resistance in advance and then subtracting them from the results.

Table 1 lists resistance value coefficients of fluctuation $\delta R_{h_i}[V]$ and their averages for applied voltages of 3 kV and 5 kV. The higher the voltage, the greater the resistance value coefficient of variation.

4.2 Calibration of the division ratio coefficient of variation $\delta k[V]$

We calibrated the division ratio coefficient of variation $\delta k[V]$ by substituting the measured resistance value coefficient of variation $\delta R_{h_i}[V]$ into the electronic circuit model.

In the domain of 1 kHz and lower for which calibrated values for $\delta k[5\text{ kV}]$ at each frequency are shown in Fig. 7, the division ratio coefficient of variation $\delta k[5\text{ kV}]$ and average value for the resistance value coefficient of variation $\delta R_{h_i}[5\text{ kV}]$ differ by 1 ppm or less, and Equation (4) applies. As a result, it is likely that the effects of parasitic capacitance are small enough to ignore in the 1 kHz and lower domain for AC voltages as well.

By contrast, in the domain of frequencies greater than 1 kHz, $\delta k[5\text{ kV}]$ and the average value for $\delta R_{h_i}[5\text{ kV}]$ diverge, as shown in Equation (5). Since the impedance of the parasitic capacitance decreases as the frequency increases, this divergence likely increases.

4.3 Uncertainty in the division ratio coefficient of variation $\delta k[V]$

(1) Identification of sources of uncertainty

Uncertainty in the division ratio coefficient of variation $\delta k[V]$ consists of uncertainty deriving from the method used to measure resistance values and uncertainty derived from the method used to build the electronic circuit model.

(2) Uncertainty deriving from the method used to measure resistance values

Uncertainty deriving from the method used to measure resistance values consists of uncertainty deriving from calibrators and uncertainty deriving from differences in heat conditions.

Table 1: Resistance value coefficients δR_{h_i} [V] of variation at 3 kV and 5 kV and their average values

Resistance No.	Resistance fluctuations	
	δR_{h_i} [3 kV] [ppm]	δR_{h_i} [5 kV] [ppm]
1	-12.8	-36.1
2	-15.9	-43.1
3	-14.9	-34.9
4	-12.5	-42.1
5	-15.3	-42.1
6	-15.4	-44.8
7	-11.4	-35.0
8	-8.9	-34.5
9	-10.6	-49.1
10	-12.5	-35.6
11	-9.6	-41.1
12	-11.1	-42.3
Average	-12.6	-40.1

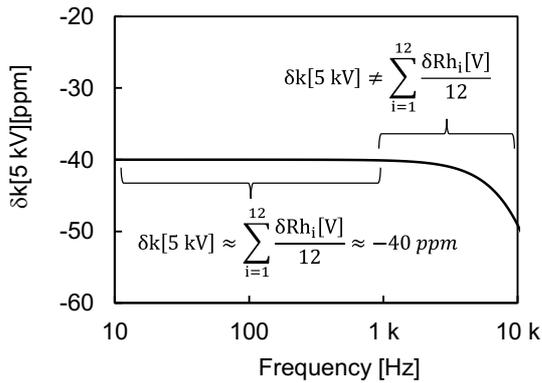


Fig. 7 Calibrated values for the division ratio coefficient of variation δk [5kV] for an applied voltage of 5 kV

We calculated uncertainty deriving from calibrators based on the specifications of the 5730A, which was used in voltage generation, and the 3458A, which was used in current measurement. We estimated standard uncertainty for the 5730A as 12 ppm, and standard uncertainty for the 3458A as 35 ppm.

Uncertainty deriving from differences in heat conditions occurs due to differences in the mounting conditions of input resistors when measuring input resistance values R_{h_i} and when using the resistors to calibrate the standard high-voltage divider. We estimated uncertainty in the resistance value coefficient of variation δR_{h_i} [5 kV] caused by these

differences in heat conditions as 49.1 ppm at most when using the resistors to calibrate the standard high-voltage divider, even assuming the worst-case scenario in which all heat thrown off by resistors on both sides is transmitted to the center resistor. We estimated standard uncertainty as 28.3 ppm, assuming a rectangular distribution.

We synthesized these uncertainty values to obtain an expanded uncertainty of 92 ppm ($k=2$) for the resistance value coefficient of variation δR_{h_i} [5 kV].

We then calculated uncertainty in the division ratio coefficient of variation δk [5kV] deriving from the method used to measure resistance values by fixing the parasitic capacitance value in the electronic circuit model and varying the δR_{h_i} [5 kV] substituted into the model within the range of the calculated uncertainty. Table 2 lists those results ((1) Uncertainty A).

(3) Uncertainty deriving from the modeling method

Although it is difficult, on a theoretical basis, to calculate uncertainty deriving from uncertainty in parasitic capacitance values in the electronic circuit model, a 50% fluctuation in parasitic capacitance, for example, causes the 10 kHz gain divergence between observed and simulated values to increase by at least 10%. Consequently, we estimated that uncertainty as 50% at most.

We then calculated uncertainty in the division ratio coefficient of variation δk [5kV] deriving from the modeling method by fixing the resistance value in the electronic circuit model and varying the parasitic capacitance value substituted into the model within the range of the calculated uncertainty. Table 2 lists those results ((1) Uncertainty B).

4.4 Summary and verification of calibration results

Table 2 summarizes calibration values for the division ratio coefficient of variation δk [5 kV] and uncertainty values for an applied voltage of 5 kV. By using this technique, the division ratio for the standard high-voltage divider at an applied voltage of 5 kV can be calibrated with an uncertainty of 351 ppm or less.

In addition, a comparative verification with a voltage transformer at 5 kV and 60 Hz (JCSS calibration

Table 2: Summary of calibration values and uncertainty values (for an applied voltage of 5 kV) In the table, “(1) Uncertainty A” represents uncertainty deriving from the method used to measure resistance values as calculated in 4.3–(2), while “(2) Uncertainty B” represents uncertainty deriving from the modeling method as calculated in 4.3–(3).

Freq. [Hz]	dk[5 kV] [ppm]	(1) Uncertainty A [ppm]	(2) Uncertainty B [ppm]	(3)=(1)+(2) Uncertainty of δk [5 kV] [ppm]	(4) Uncertainty of k[1 kV] [ppm]	(5)=(3)+(4) Uncertainty of k[5 kV] [ppm]
≤ 1 k	-40.1	92.3	0.1	92.4	152.0	244.4
2 k	-40.4	92.9	0.4	93.3	229.0	322.3
5 k	-42.7	98.1	2.7	100.8	229.0	329.8
10 k	-49.5	113.9	8.1	122.0	229.0	351.0

using JEMIC with a calibration uncertainty of 50 ppm [k=2]) found that both values matched one another closely within the uncertainty range, with a difference of 0.9 ppm.

5. VT1005 calibration using the standard high-voltage divider

5.1 VT1005 calibration method

We measured standard high-voltage divider output and VT1005 output with the 3458A and conducted a comparative calibration. A high-voltage power supply was used to generate the high voltages. For reasons related to the performance of the high-performance power supply, the calibration was performed at up to 10 kHz at 3 kV and at up to 2 kHz at 5 kV.

5.2 Results of the VT1005 calibration

Fig. 8 illustrates a comparison of calibration results (amplitude error) for the VT1005 at applied voltages of 1 kV (evaluated using the 5730A), 3 kV, and 5 kV. At 50 ppm or less at the rated 5 kV, the VT1005’s voltage dependence is sufficiently low relative to its accuracy. In this way, we were able to verify that the VT1005 provides a sufficient level of performance to accurately measure power at high voltages.

6. Summary

We developed a standard high-voltage divider and a method for calibrating it in order to define the accuracy of the VT1005 across a broad band of

frequencies for high voltages in excess of 1 kV. Following is a summary of our findings:

(1) We developed a technique for calibrating the division ratio $k[V]$ at a desired voltage V using the division ratio coefficient of variation $\delta k[V]$ based on 1 kV. We estimated uncertainty in the division ratio for the standard high-voltage divider while 5 kV is being applied—the conditions at which uncertainty reaches its peak—as 351 ppm. This technique makes possible calibration with uncertainty of 0.1% or less at frequencies other than DC and grid frequencies.

(2) We carried out high-voltage calibrations of the VT1005 at up to 10 kHz at 3 kV and at up to 2 kHz at 5 kV using the developed calibration technique. At 50 ppm or less at the rated 5 kV, the VT1005’s voltage dependence is low relative to its accuracy. Based on these results, we were able to verify that the VT1005

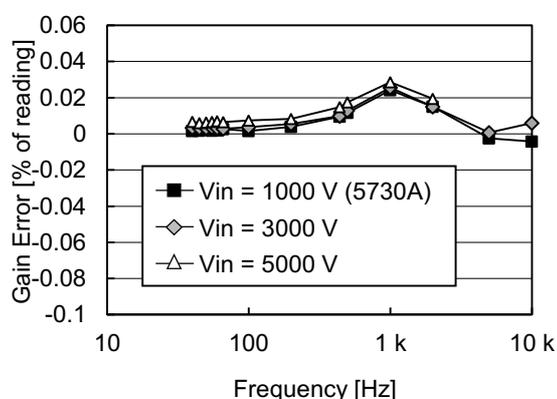


Fig. 8: VT1005 calibration results (Comparison with applied voltages of 1 kV, 3 kV, and 5 kV)

provides a sufficient level of performance for accurately measuring power at high voltages and across a broad range of frequencies. The VT1005 can be used to perform high-accuracy power measurement of high voltages in excess of 1 kV across a broad range of frequencies, a task that has been impossible to date.

7. Acknowledgments

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8. References

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Appendix 1: Derivation of Equation (4)

This discussion assumes a DC voltage. The division ratio k [V] for an applied voltage V can be expressed by Equation (X1) below. However, α represents the buffer gain ($\alpha \approx 10$).

$$k[V] = \frac{1}{\alpha} \left(\frac{\sum_{i=1}^{12} Rh_i[V] + Rl}{Rl} \right) \quad (X1)$$

Equation (X2) can be obtained from $\sum_{i=1}^{12} Rh_i[1kV] \gg Rl$, while Equations (X3) and (4) can be obtained from $Rh_1[1kV] \approx Rh_2[1kV] \approx \dots \approx Rh_{12}[1kV]$.

$$\begin{aligned} \delta k[V] &= \frac{\sum_{i=1}^{12} Rh_i[V] - \sum_{i=1}^{12} Rh_i[1kV]}{\sum_{i=1}^{12} Rh_i[1kV] + Rl} \\ &\approx \frac{\sum_{i=1}^{12} Rh_i[V] - \sum_{i=1}^{12} Rh_i[1kV]}{\sum_{i=1}^{12} Rh_i[1kV]} \quad (X2) \end{aligned}$$

$$\approx \sum_{i=1}^{12} \frac{1}{12} \left(\frac{Rh_i[V] - Rh_i[1kV]}{Rh_i[1kV]} \right) \quad (X3)$$

$$= \sum_{i=1}^{12} \frac{\delta Rh_i[V]}{12} \quad (4)$$

Appendix B: The fabricated standard high-voltage divider

Fig. X1 shows the photograph of the fabricated standard high-voltage divider.

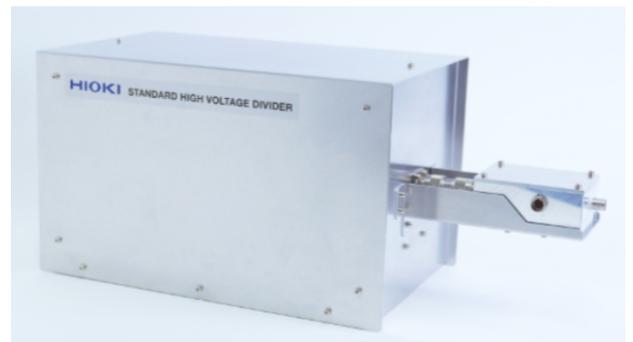


Fig. X1: The photograph of the fabricated standard high-voltage divider.