HIOKI E. E. CORPORATION

Letter of Volatility

This letter outlines the memory types and deleting methods for said memory used in the HIOKI POWER ANALYZER PW6001. Please use the contents of this letter when considering the PW6001 and its data security classification, especially in regards to data deleting.

For additional data, please contact the nearest HIOKI representative.

Volatile Memory

	Memory type	User Accessible	Backup Battery	Usage	Clearing method	Stores user data
Volatile Memory 1	CPLD	No	No	Data buffering (CPLD of input units)	Power down	Yes
Volatile Memory 2	CPLD	No	No	Data buffering (CPLD of output unit)	Power down	Yes
Volatile Memory 3	FPGA	No	No	Data buffering (FPGA of the PW6001)	Power down	Yes
Volatile Memory 4	Synchronous DRAM	No	No	Data buffering for FPGA	Power down	Yes
Volatile Memory 5	CPU	No	No	Working memory for OS, power calculation, harmonics calculation, and FFT calculation	Power down	Yes
Volatile Memory 6	Synchronous DRAM	No	No	Working memory for OS, power calculation, harmonics calculation, and FFT calculation	Power down	Yes
Volatile Memory 7	SRAM	Yes (by changing the settings) (by saving or loading settings files)	Yes*1	Backs up the settings	Initialize when the PW6001 is powering up*2	Yes
Volatile Memory 8	RTC	Yes (by setting)	Yes*1	Clock	Initialize on the system screen*3	No

*1 These memories are backed up by a powerful battery to keep settings from being lost in times of power loss. Consequently, even though these memory types are volatile and would clear when powered down, this clearing method does not work.
*2 The memory can be initialized by pressing a single button when the PW6001 is powering up. The initializing function replaces all existing bit data with that of the factory setting. There is no way of retrieving previous bit data.
*3 This is the real time clock memory. Whenever the clock is reset, all previous data is replaced with new bit data, deleting all past information.

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Non-Volatile Memory

	Memory type	User Accessible	Backup Battery	Usage	Clearing method	Stores user data
Non-Volatile Memory 1	CPLD	No	Yes	Program for CPLD inside input units	None	No*4
Non-Volatile Memory 2	CPLD	No	Yes	Program for CPLD inside output unit	None	No*4
Non-Volatile Memory 3	Flash Memory	No	Yes	Program for FPGA, CPU	None	No*4

*4 Non-Volatile memory on which user data is not saved do not have methods of erasure. This is because data security is not an issue.

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